REMARKS

The allowability of claims 22-30 is acknowledged. The reasons for allowance imply that the claimed invention was allowed because the prior art did not disclose certain limitations found in the claims. The limitations characterized by the Examiner, however, if indeed found in the prior art, would not render the claimed invention invalid under 35 USC §102 because the claimed invention includes a number of limitations not addressed in the reasons for allowance. With respect to 35 USC §103, the rigors of establishing a *prima facie* case of obviousness include not only a showing that the prior art teaches the entire claimed invention (all limitations are to be considered), but also that combining the various prior art references is suggested in the art or that there would be motivation to make the combination. Unless Applicants hear otherwise, the comments herein are, as intended, clarifying in a manner consistent with the law.

Claims 1-30 remain for consideration and are thought to be allowable over the cited art.

The Office Action does not establish that claims 1-21 are unpatentable under 35 USC §103(a) over "Balakrishnan" (US patent 6,135,647 to Balakrishnan et al.). As set forth in the previous Amendment, the rejection is traversed because a *prima facie* case of obviousness has not been established. The arguments and explanations set forth in the previous amendment are maintained in this response.

In the Examiner's Response to Arguments, the Examiner alleges that Balakrishnan's teaching of VHDL, HDL, RTL codes, and Verilog correspond to the limitations related to the processing of a first low-level design representation targeting a first integrated circuit. However, Balakrishnan's teachings indicate that each of the Examiner's cited examples is a high-level description, not a low-level description. For example, Balakrishnan's Background clearly indicates that each of VHDL, HDL, RTL codes, and Verilog are high level descriptions, not a low-level design representation (an example of a low-level design representation is a gate level description, col. 1, line 16-24). . For example, Balakrishnan at col. 1, lines 30-31: "HDLs provide a rich set of constructs to describe the functionality of a module at RTL. At this level, the

functionality is described by using high level constructs...." Thus, the limitations of the claims are not shown to be suggested by Balakrishnan. The current Office Action also fails to provide evidence to support a motivation to modify Balakrishnan, and therefore, fails to establish a *prima facie* case of obviousness.

CONCLUSION

Reconsideration and a notice of allowance are respectfully requested in view of the Remarks presented above. If the Examiner has any questions or concerns, a telephone call to the undersigned is invited.

Respectfully submitted,

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I hereby certify that this correspondence is being deposited with the United States Postal Service as first-class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on August 15, 2005.

Pat Slaback
Name

Signature